# Si3050PPT-EVB

## EVALUATION BOARD FOR THE Si3050

### Description

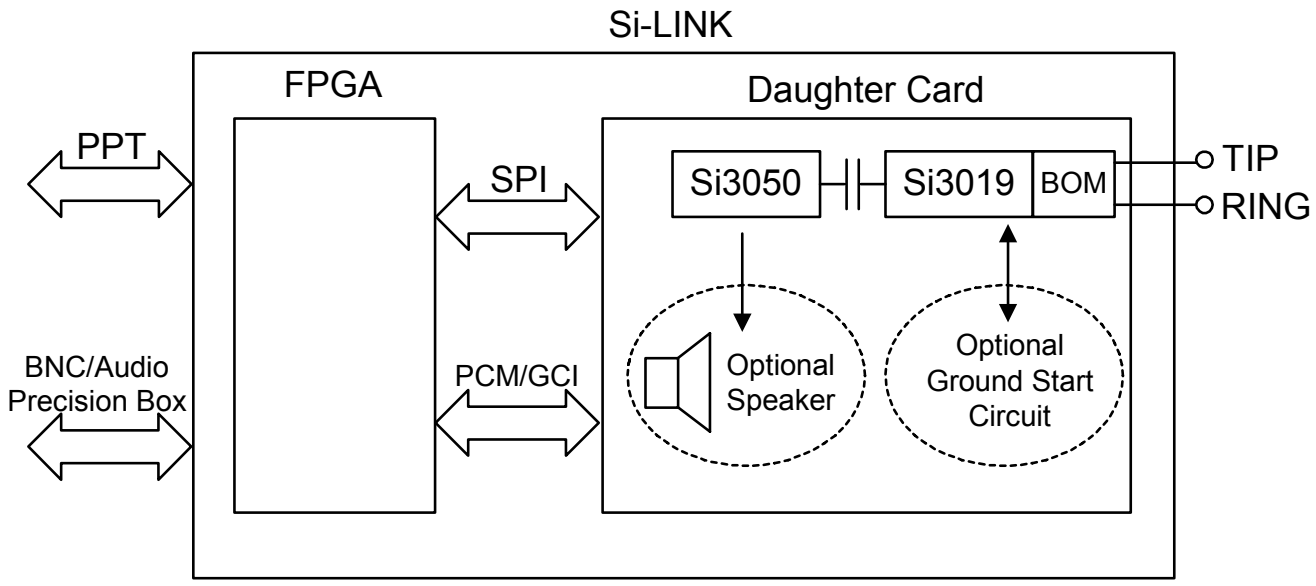
The Si3050PPT-EVB provides the telecommunications system engineer an easy way to evaluate the functionality of Silicon Laboratories' Si3050/Si3019 integrated voice direct access arrangement (DAA) solution. The Si3050 integrates an SPI, PCM, and GCI serial interface as well as system-side DAA functionality. In conjunction with the Si3019 global line-side silicon DAA chip, it provides a low-cost, solid-state, globally-compliant voice DAA solution.

The Si3050/Si3019 chipset can be easily controlled from a PC using the supplied application software.

### Features

- Ability to read and write DAA registers
- DAC waveform generation from a series of standard waveforms or from a .wav file
- ADC data capture and display in either time or frequency domain
- Recommended layout for key components
- Daisy-chain support

### Function Block Diagram



# 1. Functional Description

The Si3050PPT-EVB provides the telecommunications system engineer an easy way to evaluate the Si3059/19 solution. Silicon Labs' DAAs are integrated direct access arrangements that provide a digital, low-cost, solid-sate interface to worldwide telephone lines. Through the patented ISOcap™ technology, the Si3050/19 eliminates the need for an analog frond end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid.

The Si3050PPT-EVB also supports the connection of multiple devices on an SPI/PCM interface. The evaluation board provides a straightforward means of evaluating this feature.

The evaluation board consists of the Si3050PPT-EVB Si-LINK (mother) board and the Si3050DC-EVB daughter card. A custom ribbon cable is also provided to connect to the parallel port of a PC. Contact a Silicon Laboratories representative for more information.

## 1.1. Motherboard-Daughter Card Connection

Si3050DC-EVB connects to the Si3050PPT-EVB through five sockets, JS1–JS5. JS1 is a 5x2 socket and JS2 is a 2x2 socket connecting SPI digital signals of the Si3050. JS3 is a 5x2 socket connection reserved for future use. JS4 is a 5x2 socket connection that routes the Vdd regulated supply. JS5 is a 5x2 socket connection to the PCM digital signals of the Si3050. JS3 is a no-connect in this application.

## 1.2. Power Supply

Power is supplied to the EVB by means of J1 and J4. J4 is a 2.1 mm power jack that allows the use of a wall transformer. A 9 V supply/300 mA is typically used, but the on-board voltage regulator will also work with a dc voltage between 7.5 V and 20 V. A diode bridge is used to correct polarity. The on-board regulator, U7, provides 5 V to the call progress circuit, the on-board oscillator, and other boards daisy chained to the Si3050PPT-EVB. This 5 V is further regulated to 3.3 V to power the daughter card and the input/output ports of the FPGA. A third regulator provides 2.5 V for the core voltage of the FPGA. J1 is a no-connect in this application.

## 1.3. Clock Generation

The Si3050 requires an FSYNC, PCLK, and SCLK input. An on-board oscillator (Y1) is used by the FPGA to clock all the subsystems as well as generate and provide the FSYNC, PCLK, and SCLK to the DAA. FPGA is designed to use a 32.768 MHz oscillator (included with the board).

## 1.4. Reset Circuit

The Si3050/19 requires an active low pulse on $\overline{\text{RESET}}$ following power up and whenever all registers need to be reset. For development purposes, the Si3050PPT-EVB includes a reset push button, SW1, that is used by the FPGA to generate a reset pulse of the DAA.

## 1.5. Line Connection

J1 is provided to connect the EVB to a standard RJ-11 connector. The system cannot execute an off-hook command without the phone line connected.

## 1.6. PC Parallel Port

JP2 and P3 connect through the Silicon Labs custom ribbon cable to the parallel port of the PC. The parallel port connection allows the designer to read and write the DAA registers using the evaluation software included with the Si3050PPT-EVB.

## 2. Configuring the Si-LINK

The Si-LINK motherboard is used to interface the Si3050 to a PC or other audio system for easy evaluation. It uses an FPGA to translate the parallel port interface to either SPI/PCM, SPI-only, or GCI to communicate with the Si3050.

When in SPI/PCM mode, the PCM audio data and SPI control data are communicated from the controlling PC using the aforementioned software. This mode allows the user to evaluate the DAA without any lab equipment other than a PC.

By selecting SPI-only operation, the PC is still used to control the DAA through the SPI bus, but the PCM audio data is routed from an external source. This external source may be an Audio Precision system using the P1 and P2 headers or a PCM highway using the BNC connectors, J5–J8 (not populated).

To evaluate the Si3050's operation with the GCI interface, the PC may be used to send the audio data and control. The FPGA performs the necessary translation to communicate to the Si3050 in this mode.

The fourth mode of operation is the pass-thru mode. In this mode, the FPGA is only used to route the GCI bus to the Audio Precision or BNC headers on the Si-LINK board. In this mode, a PC is not required to control the evaluation platform.

| Mode | JP3 (Source) | JP4 (Format) |
|---|---|---|
| SPI/PCM | 0 | 0 |
| SPI-Only | 1 | 0 |
| GCI | 0 | 1 |
| Pass-Thru | 1 | 1 |

## 3. Configuring the Si3050DC-EVB

The Si3050DC-EVB has six jumpers. The first five control the boot-strap options for configuring the Si3050. The default state is set to allow the Si3050 to be controlled using the SPI bus. See Figure 1.

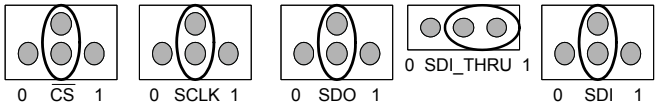



**Figure 1. SPI Control Mode Default State**

By changing the jumper configuration prior to powering the board, the mode of the board can be set according to Tables 1–3.

JP10 is the sixth jumper on the Si3050DC-EVB. Moving this jumper to the $\overline{\text{INT}}$ position routes pin 9 of the Si3050 to the Si-LINK motherboard. When the jumper is in the AOUT position, this signal is routed to the optional call progress speaker system, which is not populated by default on the evaluation platform. Refer to the AOUT PWM circuit in the Si3050 data sheet for values used to populate this circuit.

**Table 1. PCM or GCI Highway Mode Selection**

| SCLK | SDI | Mode Selected |
|---|---|---|
| 1 | X | PCM Mode |
| 0 | 0 | GCI Mode, B2 Channel used |
| 0 | 1 | GCI Mode, B1 Channel used |

**Note:** Values shown are the states of the pins at the rising edge of RESET.

**Table 2. Pin Functionality in PCM or GCI Highway Mode**

| Pin Name | PCM Mode | GCI Mode |
|---|---|---|
| SDI_THRU | SPI Data Through-put pin for Daisy Chaining Operation (Connects to the SDI pin of the subse-quent device in the daisy chain) | Sub-frame Selector, bit 2 |
| SCLK | SPI Clock Input | PCM/GCI Mode Selector |
| SDI | SPI Serial Data Input | B1/B2 Channel Selector |
| SDO | SPI Serial Data Out-put | Sub-frame Selector, bit 1 |
| $\overline{\text{CS}}$ | SPI Chip Select | Sub-frame Selector, bit 0 |
| FSYNC | PCM Frame Sync Input | GCI Frame Sync Input |
| PCLK | PCM Input Clock | GCI Input Clock |
| DTX | PCM Data Transmit | GCI Data Transmit |
| DRX | PCM Data Receive | GCI Data Receive |

**Note:** This table denotes pin functionality after the rising edge of RESET and mode selection.

**Table 3. GCI Mode Sub-Frame Selection**

| | SDI_THRU | SDO | $\overline{CS}$ |
|---|---|---|---|
| GCI Subframe 0 Selected (Voice channels 1–2) | 1 | 1 | 1 |
| GCI Subframe 1 Selected (Voice channels 3–4) | 1 | 1 | 0 |
| GCI Subframe 2 Selected (Voice channels 5–6) | 1 | 0 | 1 |
| GCI Subframe 3 Selected (Voice channels 7–8) | 1 | 0 | 0 |
| GCI Subframe 4 Selected (Voice channels 9–10) | 0 | 1 | 1 |
| GCI Subframe 5 Selected (Voice channels 11–12) | 0 | 1 | 0 |
| GCI Subframe 6 Selected (Voice channels 13–14) | 0 | 0 | 1 |
| GCI Subframe 7 Selected (Voice channels 15–16) | 0 | 0 | 0 |

# 4. Evaluation Software

The Si3050PPT-EVB includes an easy-to-use graphical interface for controlling the evaluation platform. This software allows the system designer to characterize the Si3050 DAA performance without constructing any custom hardware. The evaluation software includes the following features:

- Ability to read and write DAA registers using the SPI or GCI bus
- DAC waveform generation from a series of standard waveforms or from a .wav file
- ADC data capture and display in either the time or frequency domain using either PCM or GCI bus
- Daisy-chain support
- Transmit and receive path attenuation and gain settings
- Ring detection
- Loop current measurement

## 4.1. PC System Requirements

The application software for the Si3050PPT-EVB has the following system requirements:

- Windows98®, Windows2000®, or WindowsXP®
- Available parallel port
  - EPP or ECP parallel port mode for Windows 98®
  - EPP parallel port mode for Windows 2000® and WindowsXP®
- 450 MHz Pentium II® or greater recommended
- 64 MB of memory or greater recommended

## 4.2. Installation

The supplied CD contains the Si3050PPT-EVB windows driver files as well as a setup utility for installing the evaluation software.

To install the Si3050PPT-EVB software, run the installation program on the "Silicon Laboratories Wireline Software CD." The path for the installation program is Si3050 Evaluation Software\setup.exe. The installer guides the user through the installation process for Si3050PPT-EVB.exe and the LabVIEW Run-Time engine.

# 5. Using the Si3050PPT-EVB Application Software

A shortcut for starting the application software that controls the Si3050PPT-EVB is installed in the Windows Start Menu under the Programs folder in the "Si3050 Evaluation Software" folder.

## 5.1. Application Menus

Three pulldown menus are used to configure the operation of the software:

- **Run**:
  - Exit: Stops the program
  - Save: Stores the audio waveform into .wav files
- **Configure**:
  - Configure DAA: Display hardware status and user configuration. User can set advanced software options.
  - Reset DAA: Resets DAA and executes basic initialization sequences on Reg 1, Reg 5–7, Reg 33–37, and Reg 42
- **Design Tool**
  - Register Map: Displays Register Map of Si3050
  - Signal Flow Diagram: Displays Signal Flow Diagram of Si3050 and Si3019.
  - Transhybrid Loss Calculation: Calculate transhybrid loss over frequency
  - Ringing: Help user program ring validation registers.
- **Help**: Displays information about the evaluation board

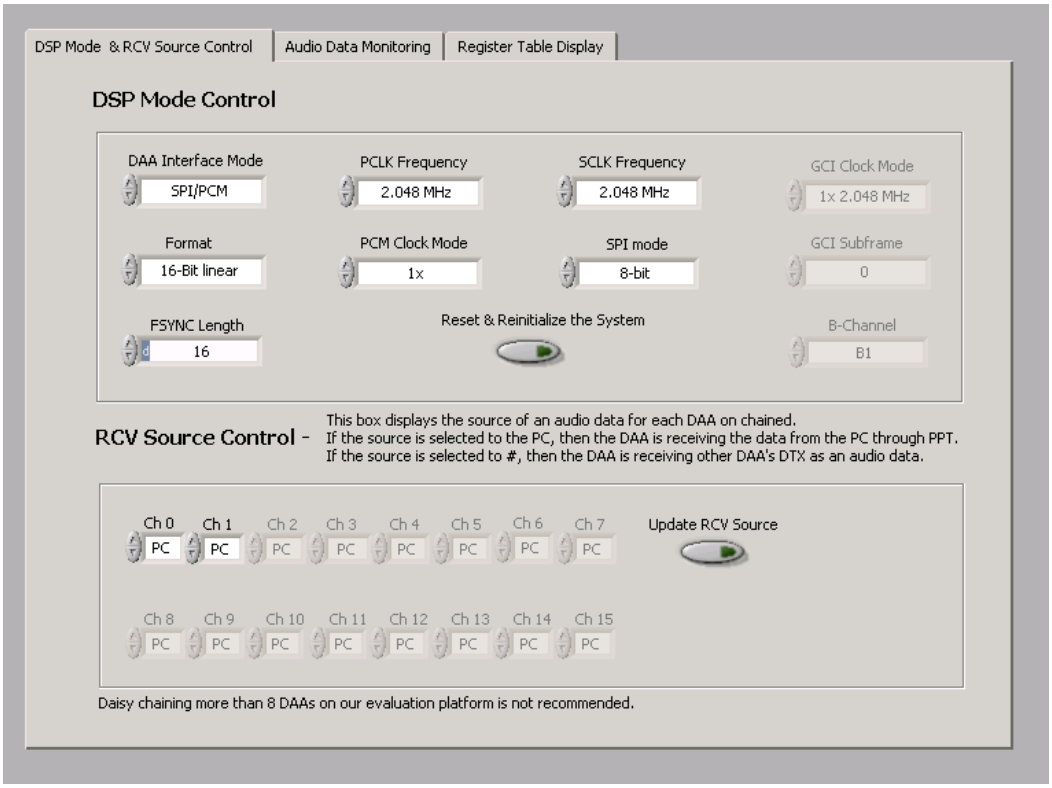



**Figure 2. Si3050PPT-EVB Evaluation Software in the DSP Mode Control and RCV Source Control View**

## 5.2. DSP Mode and RCV Source Control View

The user interface in the DSP Mode and RCV Source Control view for the Si3050PPT_EVB software is shown in Figure 2. This figures shows the DAA's mode of communication and RCV source for each channel when the application is launched.

### DSP Mode Control

DSP mode control is described in the following list:

- **Format**: Selects the format of the audio data to be transmitted over PCM or GCI bus. By changing the format, the software will automatically execute a write to DAA Register 33 PCMF bits or DAA Register 44 GCIF bits.
- **DAA Interface Mode**: Selects the mode of operation of the DAA from SPI/PCM, SPI/BNC, GCI, or GCI/BNC. Upon startup, this mode will reflect the "format" and "source" jumper selection on the SiLink (mother) board. The selection made via the jumper can be overwritten here.
- **PCM Clock Mode**: Selects the clock mode of PCM from 1x to 2x.
- **PCLK Frequency**: Selects the frequency of the PCLK in PCM mode from 256 kHz to 8.192 MHz in power of 2.
- **SCLK Frequency**: Selects the frequency of the SCLK from 256 kHz to 8.192 MHz in power of 2.
- **SPI Mode**: Selects the length of $\overline{CS}$ to either 8-bit or 16-bit.
- **GCI Clock Mode**: Selects the frequency and clock mode of PCLK in GCI mode from either 1x 2.048 MHz or 2x 4.096 MHz.
- **GCI Subframe**: Selects the subframe in GCI mode with which to communicate.
- **B-Channel**: Selects the B channel desired during GCI communication.

Changes in the DSP Mode panel will not take effect until assertion of the "Reset & Reinitialize the System" button.

### 5.2.1. RCV Source Control

RCV Source Control utilizes the daisy-chain capability of the DAA in SPI/PCM communication mode. RCV source determines the source of audio data for each device on the SiLink board.

Changes in RCV source will not take effect until assertion of the "Update RCV Source" button.

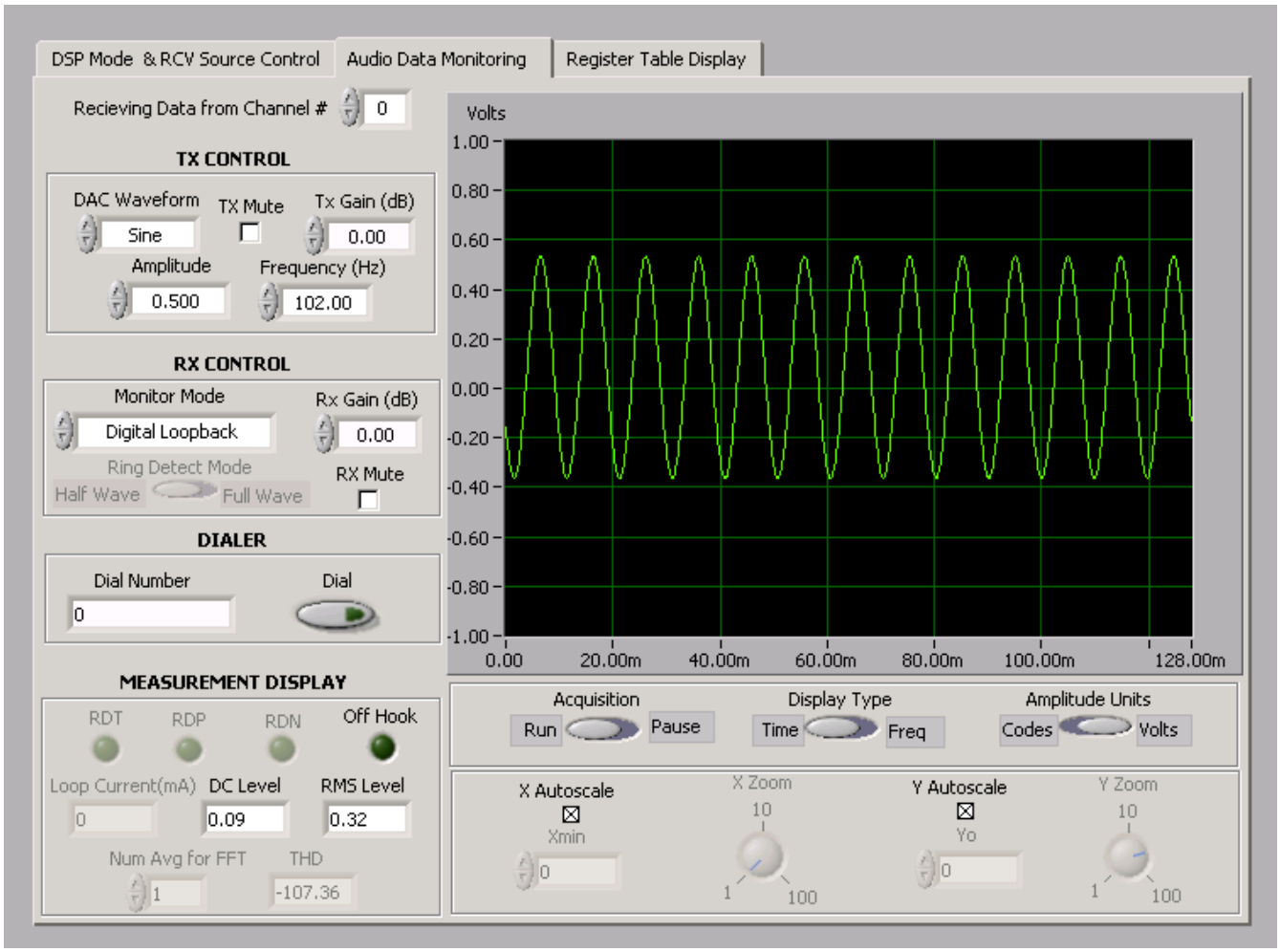



**Figure 3. Si3050PPT-EVB Evaluation Software in the Audio Data Monitoring View**

## 5.3. Audio Data Monitoring View

The audio data monitoring view is discussed in the following sections.

### 5.3.1. Receive Audio Data of Channel#

Allows selection of channel to control and view. The Audio Data Monitoring view allows the generation of DAC data and the capture and display of ADC data. Operation of the front panel in Line Monitoring view is detailed in the following list. See Figure 3.

### 5.3.2. TX Control

- **DAC Waveform**: Selects the waveform to be generated by the DAC. The waveform types are as follows: dc, Sine, Square, Ramp, and .wav file.
- **TX Gain (dB)**: Selects the transmit path gain/ attenuation.
- **TX Mute:** Mutes the transmit path
- **Amplitude**: Sets the amplitude of the DAC waveform in either volts or the units of DAC codes. The units are determined by the Amplitude Units control.
- **Frequency**: Selects the frequency (Hz) of the waveform to generate. The actual waveform frequency may vary slightly from the entered value. This variation is due to the requirement to fit an integer number of samples into the transmit buffer. The control is updated to reflect the actual waveform frequency generated. The equation for calculating the frequency of the waveform is as follows:

  Actual Frequency = round ((Waveform Frequency/DAC Sample Rate) x BufferSize) x (DAC Sample Rate/ BufferSize)

### 5.3.3. RX Control

- **Monitor Mode**: Allows the selection of several data modes. Digital Loopback mode routes the DAC data back to the receive path. On-hook mode configures the DAA to the on-hook mode. Off-hook mode configures the DAA to the off-hook mode. On-hook

line monitoring mode configures the DAA to the line monitoring state.

- **RX Gain (dB):** Selects the receive path gain/ attenuation.
- **RX Mute:** Mutes the receive path
- **Ring Detect Mode:** Allows selection of full-wave or half-wave ring detection.

#### 5.3.4. Dialer

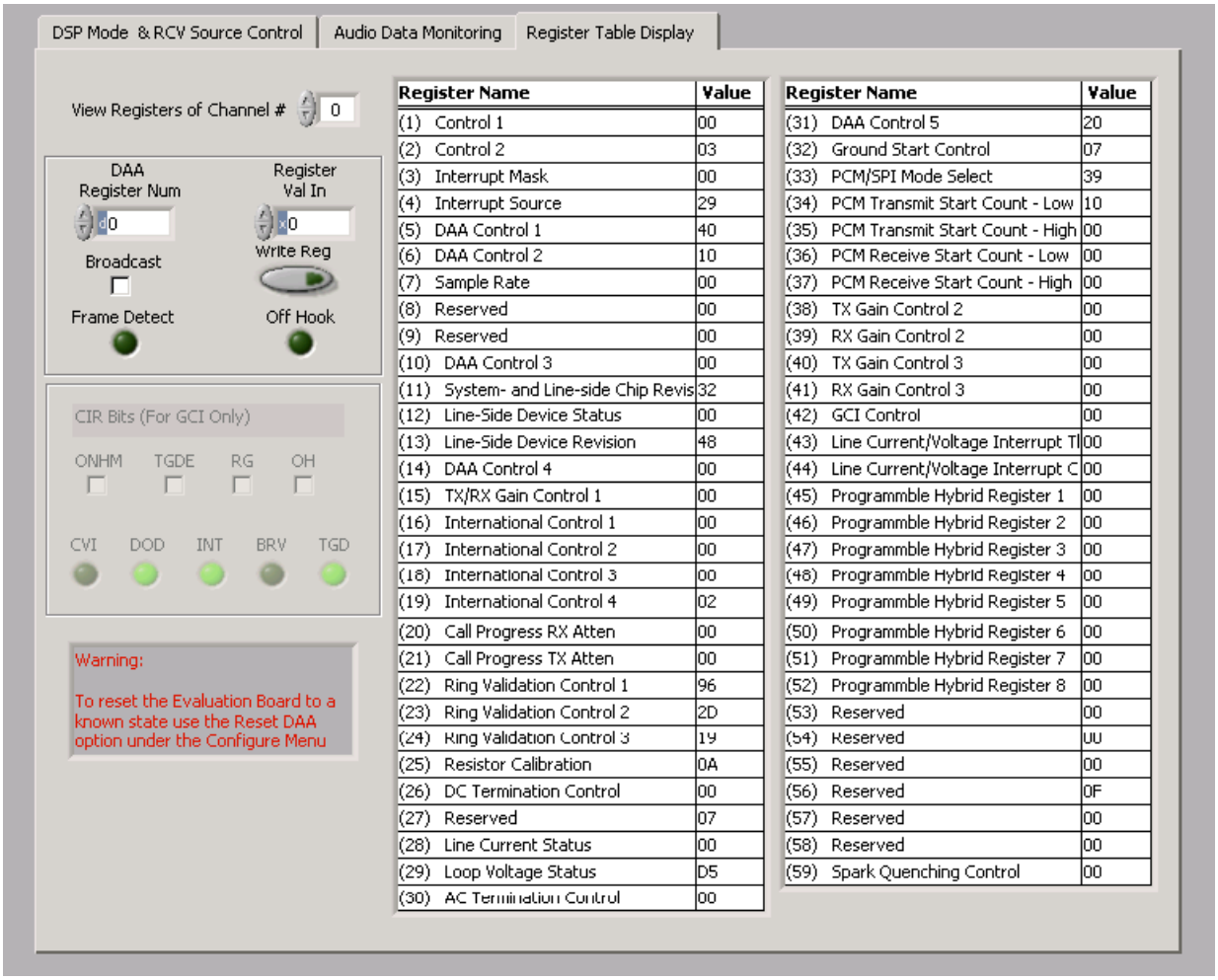
- **Dial Number:** Inputs dial number
- **Dial:** Executes dial

#### 5.3.5. Measurement

- **Loop Current**: Displays the loop current when in off-hook mode.
- **Ring Detect Bits**: Displays the state of the ring detect bits when in on-hook mode.
- **Off-Hook**: Indicates that the DAA is in the off-hook state.
- **DC Level/SINAD**: Displays either the dc level of the time domain waveform or the SINAD of the frequency domain waveform.
- **RMS Level/Frequency**: Displays either the rms level of the time domain waveform or the frequency of the largest peak in the frequency domain waveform.
- **Num Avg for FFT**: When in FFT display, the software will automatically average waveforms. This panel selects the number of averages to take.

#### 5.3.6. Wave Display Controls

- **Display Type**: Selects how the ADC data is displayed on the Waveform Graph (time or frequency domain).
- **Amplitude Units**: Sets the amplitude units for the Waveform Graph and Amplitude control to either volts or codes.
- **Acquisition**: Used to run or pause the codec data stream. Upon pausing the acquisition of the data, it displays measurement values regardless of the status of “display measurement” under the Configure menu.
- **X Autoscale**: Automatically scales the X-axis of the graph to fit the entire waveform.
- **Y Autoscale**: Automatically scales the Y-axis to fit the entire vertical range of the waveform.
- **Xmin**: Sets the origin of the X-axis when X Autoscale is disabled.
- **X Zoom**: Used to zoom a portion of the displayed waveform when X Autoscale is disabled. The waveform starts at Xmin and 1/X Zoom of the total waveform is displayed.
- **Yo**: Sets the origin of the Y-axis when Y Autoscale is disabled. Half of the waveform is displayed above Yo, and half is displayed below Yo.




| Register Name | Value |
|---|---|
| (1) Control 1 | 00 |
| (2) Control 2 | 03 |
| (3) Interrupt Mask | 00 |
| (4) Interrupt Source | 29 |
| (5) DAA Control 1 | 40 |
| (6) DAA Control 2 | 10 |
| (7) Sample Rate | 00 |
| (8) Reserved | 00 |
| (9) Reserved | 00 |
| (10) DAA Control 3 | 00 |
| (11) System- and Line-side Chip Revis | 32 |
| (12) Line-Side Device Status | 00 |
| (13) Line-Side Device Revision | 48 |
| (14) DAA Control 4 | 00 |
| (15) TX/RX Gain Control 1 | 00 |
| (16) International Control 1 | 00 |
| (17) International Control 2 | 00 |
| (18) International Control 3 | 00 |
| (19) International Control 4 | 02 |
| (20) Call Progress RX Atten | 00 |
| (21) Call Progress TX Atten | 00 |
| (22) Ring Validation Control 1 | 96 |
| (23) Ring Validation Control 2 | 2D |
| (24) Ring Validation Control 3 | 19 |
| (25) Resistor Calibration | 0A |
| (26) DC Termination Control | 00 |
| (27) Reserved | 07 |
| (28) Line Current Status | 00 |
| (29) Loop Voltage Status | D5 |
| (30) AC Termination Control | 00 |

| Register Name | Value |
|---|---|
| (31) DAA Control 5 | 20 |
| (32) Ground Start Control | 07 |
| (33) PCM/SPI Mode Select | 39 |
| (34) PCM Transmit Start Count - Low | 10 |
| (35) PCM Transmit Start Count - High | 00 |
| (36) PCM Receive Start Count - Low | 00 |
| (37) PCM Receive Start Count - High | 00 |
| (38) TX Gain Control 2 | 00 |
| (39) RX Gain Control 2 | 00 |
| (40) TX Gain Control 3 | 00 |
| (41) RX Gain Control 3 | 00 |
| (42) GCI Control | 00 |
| (43) Line Current/Voltage Interrupt Tl | 00 |
| (44) Line Current/Voltage Interrupt C | 00 |
| (45) Programmble Hybrid Register 1 | 00 |
| (46) Programmble Hybrid Register 2 | 00 |
| (47) Programmble Hybrid Register 3 | 00 |
| (48) Programmble Hybrid Register 4 | 00 |
| (49) Programmble Hybrid Register 5 | 00 |
| (50) Programmble Hybrid Register 6 | 00 |
| (51) Programmble Hybrid Register 7 | 00 |
| (52) Programmble Hybrid Register 8 | 00 |
| (53) Reserved | 00 |
| (54) Reserved | 00 |
| (55) Reserved | 00 |
| (56) Reserved | 0F |
| (57) Reserved | 00 |
| (58) Reserved | 00 |
| (59) Spark Quenching Control | 00 |

**Figure 4. Si3050PPT-EVB Evaluation Software in the Register Table Display View**

## 5.4. Register Table Display View

The DAA Register view allows the Si3050 DAA registers to be read or written. The user interface for the DAA Register view is shown in Figure 4. Operation of the front panel in the DAA Register view is detailed in the following list:

- **Table**: This table displays the contents of the Si3050 DAA registers in realtime.
- **DAA Reg Num**: The Si3050 DAA register number to write (in decimal).
- **DAA Reg Value**: The contents to write to the register selected by the DAA Reg Num control (in hexadecimal).
- **Write DAA Regs**: Causes the contents of the DAA Reg Value control to be written to the DAA Reg Num register.
- **Broadcast**: Turns on the broadcast bit (SPI only).
- **FDT**: Shows the status of FDT bit, which indicates the Si3050 is communicating with the Si3019.
- **Off-Hook**: Shows the status of the off-hook bit, DAA Register 5, bit 1.
- **CIR Bits**: Allows writing and reading of CIR bits. (GCI only).

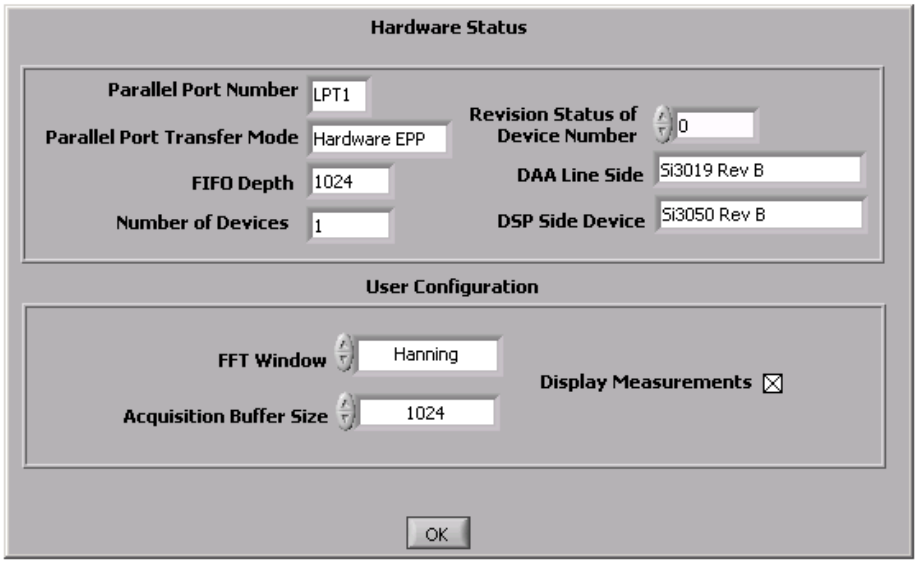



**Figure 5. Configure DAA Panel**

## 5.5. Advanced Configuration

Advanced configuration of the application software is accomplished by using the “Configure DAA” selection in the “Configure” menu. The configuration panel is shown in Figure 5. The panel contents are detailed in the following list:

- **FFT Window**: The FFT window applied to the time domain data before calculating the FFT.
- **Acquisition Buffer Size**: This is the size of the buffer, in samples, that is acquired and displayed on the Line Monitoring mode waveform graph. The buffer size can be set to between 1024 and 65536 samples in increments of 512 samples.
- **Display Measurement**: Takes realtime measurements of audio waveform.

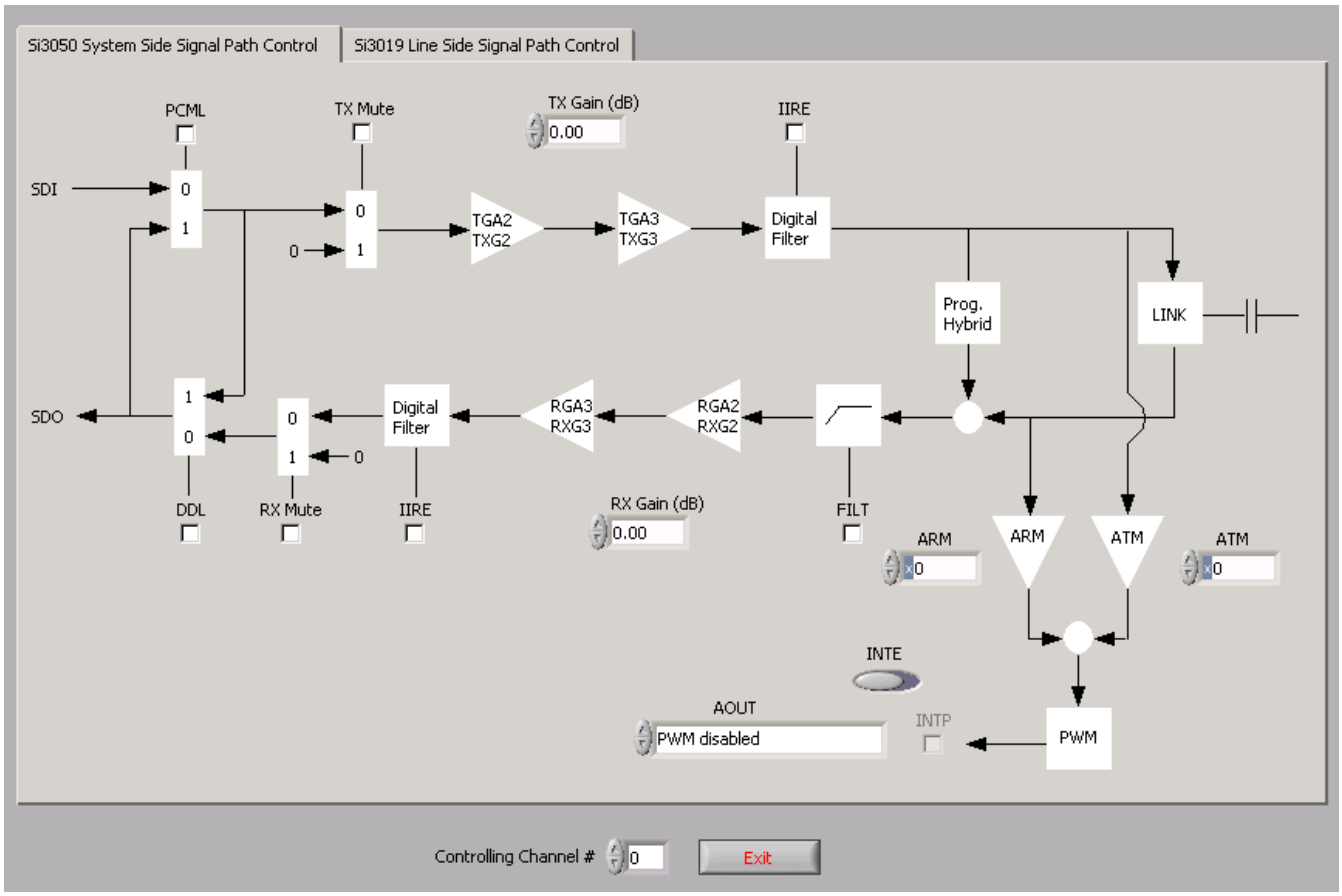



**Figure 6. Si3050 Signal Flow Diagram**

## 5.6. Signal Flow Diagrams

The signal flow diagrams of the application software shown in Figure 6 on page 11 and Figure 7 on page 12 assist users with programming DAA.

## 5.7. Si3050 Signal Path Control

- **PCML:** Turns on/off the PCML bit on DAA Register 33, bit 7
- **TX Mute:** Turns on/off the TXM bit on DAA Register 15, bit 7
- **TX Gain:** Writes to TGA2, TXG2, TGA3, and TXG3 on DAA Register 38 and 40
- **IIRE:** Turns on/off IIRE bit on Register 16, bit 4
- **DDL:** Turns on/off DDL bit on Register 10, bit 1
- **RX Mute:** Turns on/off RXM bit on Register 15, bit 0
- **RX Gain:** Writes to RGA2, RXG2, RGA3, and RXG3 on DAA Register 39 and 41
- **FILT:** Turns on/off FILT bit on Register 31, bit 1
- **ARM:** Writes to ARM on Register 20
- **ATM:** Writes to ATM on Register 21
- **INTE:** Turns on/off INTE bit on Register 2, bit 7
- **INTP:** Turns on/off INTP bit on Register 2, bit 6
- **AOUT:** Writes to PWMM and PWEM on Register 1 Si3019 Signal Path Control

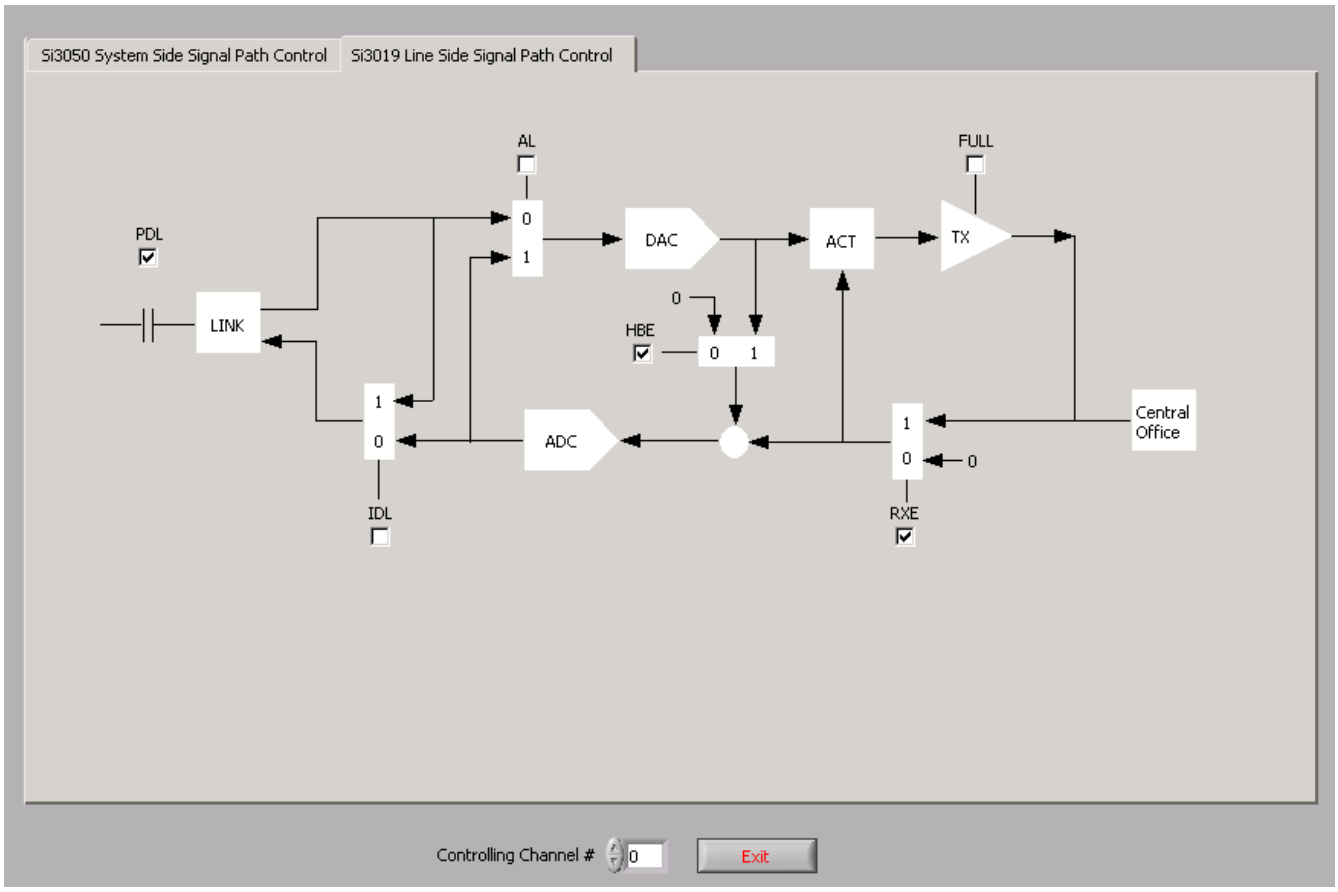



**Figure 7. Si3019 Signal Flow Diagram**

## 5.8. Si3019 Signal Path Control

- **AL:** Turns on/off AL bit on Register 2, bit 3
- **HBE:** Turns on/off HBE bit on Register 2, bit 1
- **RXE:** Turns on/off RXE bit on Register 2, bit 0
- **IDL:** Turns on/off IDL bit on Register 1, bit 1
- **PDL:** Turns on/off PDL bit on Register 6, bit 4
- **FULL:** Turns on/off FULL bit on Register 31, bit 7

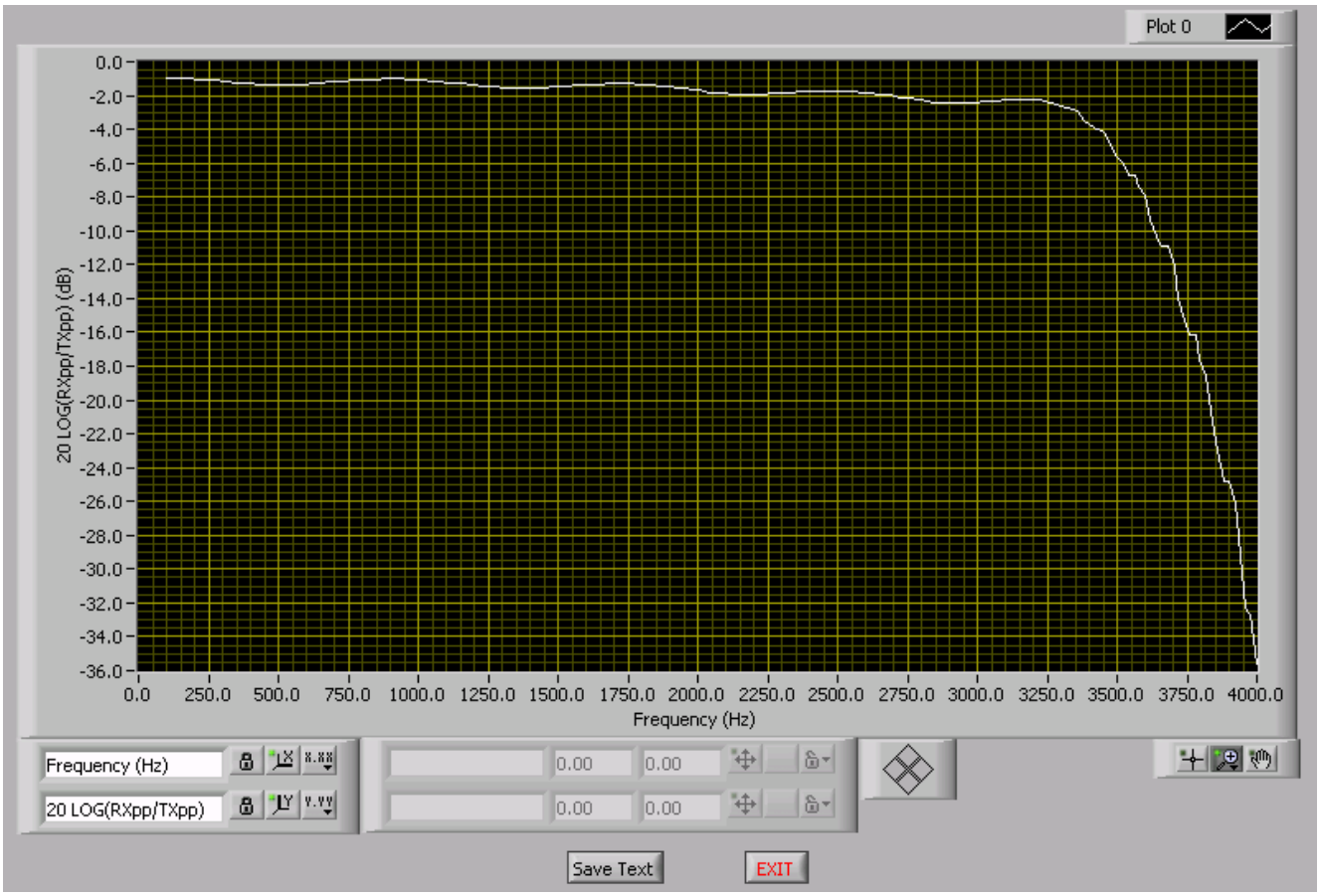



**Figure 8. Transhybrid Loss**

## 5.9. Transhybrid Loss Calculation

When “Transhybrid Loss Calculation” is selected, the Si3050PPT-EVB software will drive a signal with different frequencies and measure the transhybrid loss based on the following equation: TL = 20Log(TXpk-pk/RXpk-pk). Frequencies used to measure this start from100 Hz to 4000 Hz in 20 Hz steps.

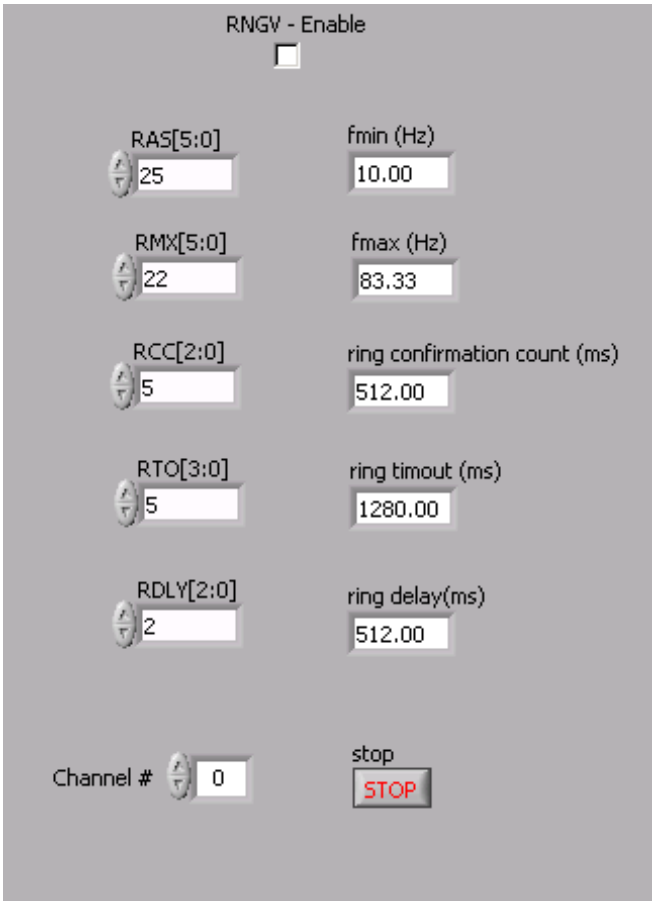



**Figure 9. Ringing**

## 5.10. Ringing

- RNGV-Enable: Turns on/off RNGV bit on Register 24, bit7
- RAS[5:0]: Update RAS bits on Register 24
- RMX[5:0]: Update RMX bits on Register 22
- RCC[2:0]: Update RCC bits on Register 23
- RTO[3:0]: Update RTO bits on Register 23
- RDLY[2:0]: Update RDLY bits on Register 22 & 23
- Fmin(Hz): Calculate fmin based on RAS bits
- Fmin(Hz): Calculate fmax based on RAS bits and RMX bits
- Ring confirmation count (ms): Shows ring confirmation count based on RCC bits
- Ring timeout(ms): Displays ring timeout based on RTO bits
- Ring delay(ms): displays ring delay based on RDLY bits

# 6. Typical Application Diagram

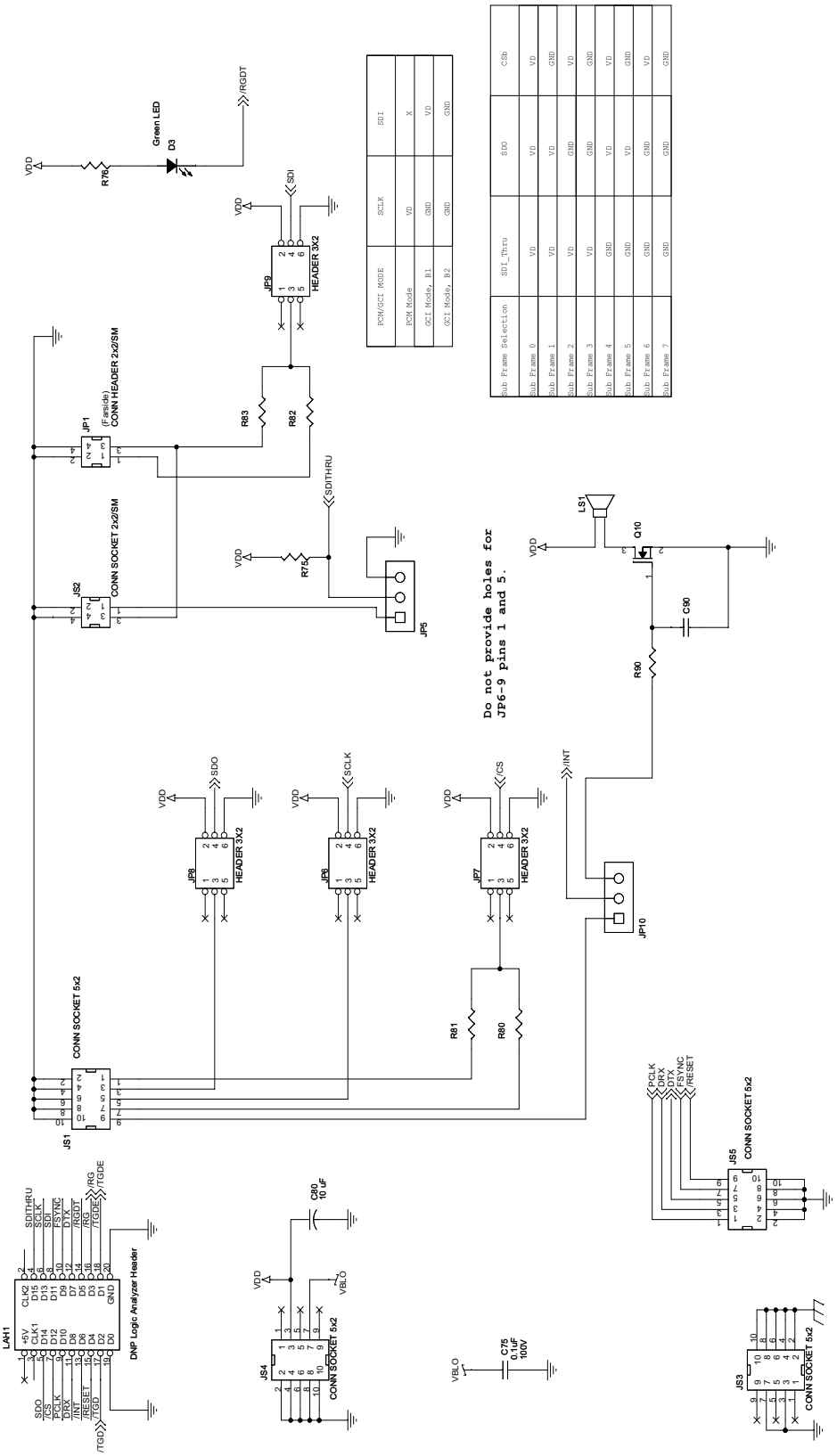



**Figure 10. Si3050-EVB Daughter Card Typical Application Circuit (1 of 4)**

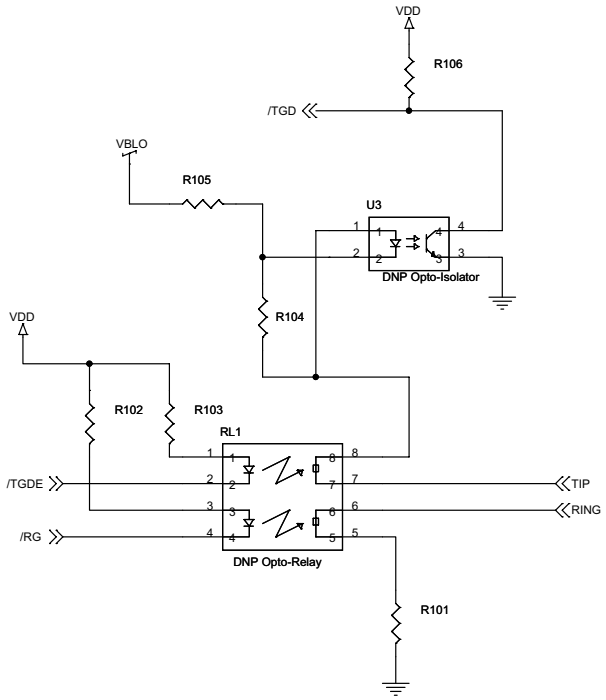



**Figure 11. Si3050-EVB Daughter Card Typical Application Circuit (2 of 4)**

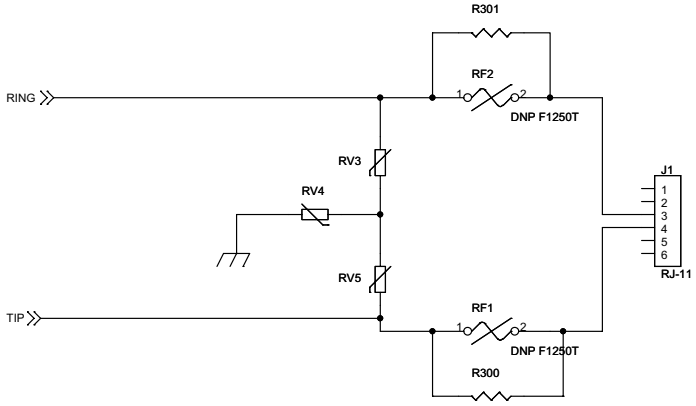



**Figure 12. Si3050-EVB Daughter Card Typical Application Circuit (3 of 4)**

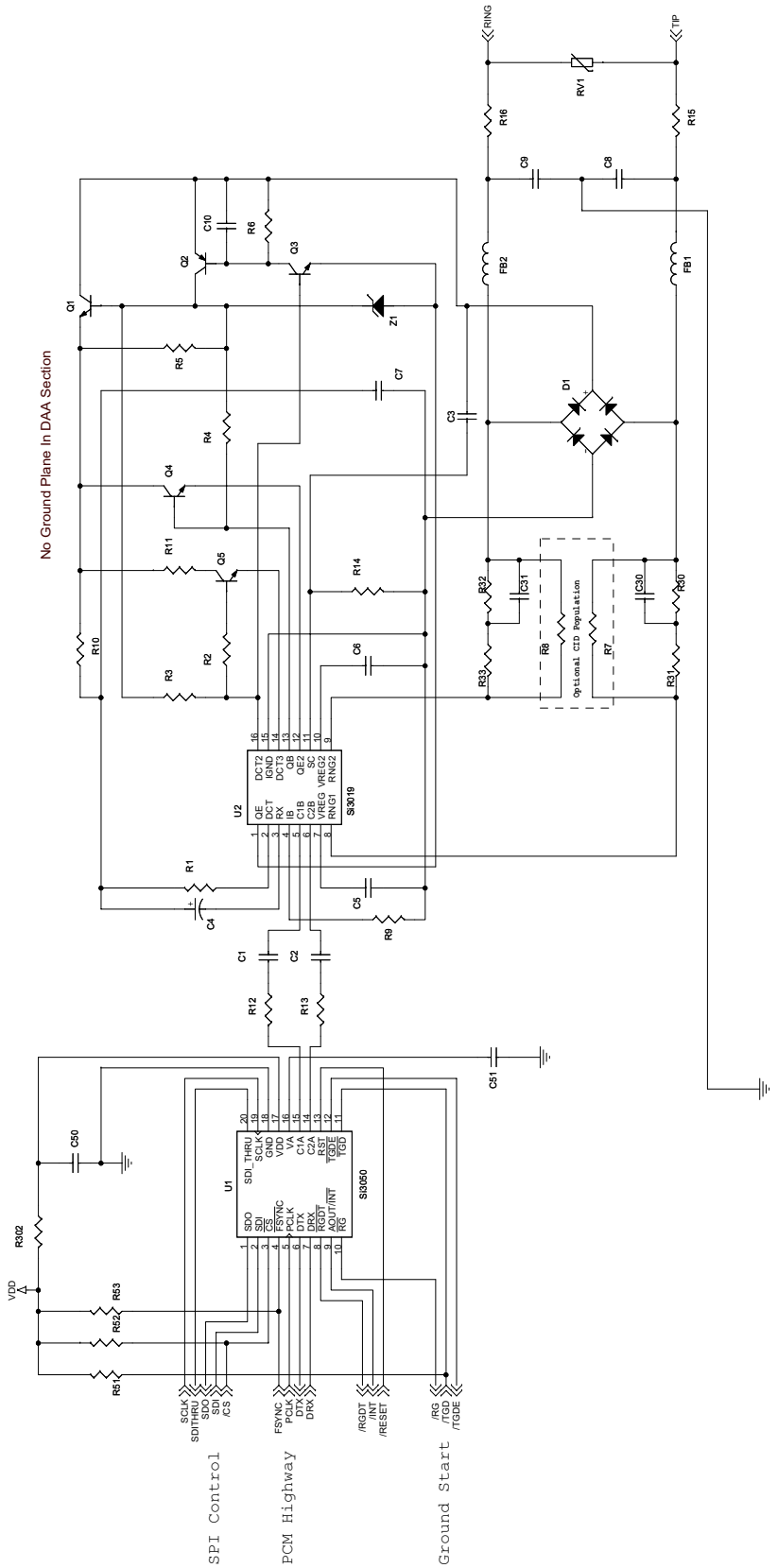



**Figure 13. Si3050-EVB Daughter Card Typical Application Circuit (4 of 4)**

## 7. Bill of Materials: Si3050PPT-EVB Daughter Card

| Item | QTY | Reference | Value | Tolerance | Rating | Part Number | Manufacturer | PCB Footprint |
|---|---|---|---|---|---|---|---|---|
| 1 | 2 | C1,C2 | 33 pF | ±20% | Y2 | GA342D1XGF330JY02L | Murata | 1808 |
| 2 | 1 | C3 | 3.9 nF | ±20% | 250 V | C0805X7R251-392MNE | Venkel | 805 |
| 3 | 1 | C4 | 1.0 uF | ±20% | 50 V | ECE-V1HS010SR | Panasonic | Size A |
| 4 | 4 | C5,C6,C50,C51 | 0.1 uF | ±20% | 16 V | C0603X7R160-104MNE | Venkel | 603 |
| 5 | 1 | C7 | 2.7 nF | ±20% | 50 V | C0603X7R500-272MNE | Venkel | 603 |
| 6 | 2 | C9,C8 | 680 pF | ±10% | Y3 | GA342DR7GD681KW02L | Murata | 1808 |
| 7 | 1 | C10 | 0.01 uF | ±20% | 16 V | C0603X7R160-103MNE | Venkel | 603 |
| 8 | 2 | C30,C31 | 120pF | ±10% | 250 V | C0805X7R251-121KNE | Venkel | 805 |
| 9 | 1 | C75 | 0.1uF | ±20% | 100V | C1206X7R101-104MNE | Venkel | 1206 |
| 10 | 1 | C80 | 10 uF | ±20% | 16 V | ECE-A16Z10 | Panasonic | radial 5x11 |
| 12 | 1 | D1 | HD04 | | 400 V | HD04-T | Diodes, Inc. | Mini-DIP |
| 13 | 1 | D3 | Green LED | | | SSF-LXH103LGD | Lumex | Thru-Hole |
| 14 | 2 | FB1,FB2 | Ferrite Bead | | | BLM21A601S | MuRata | 805 |
| 15 | 1 | JP1 | CONN HEADER 2x2/SM | | | TSM-102-02-T-DV | Samtec | SMD 2x2 100 mil |
| 16 | 2 | JP5,JP10 | 3X1 Header | | | 517-6111TN | Mouser | 3x1 100 mil |
| 17 | 4 | JP6,JP7,JP8,JP9 | HEADER 3X2 | | | 517-6121TN | Mouser | 3x2 100 mil |
| 18 | 4 | JS1,JS3,JS4,JS5 | CONN SOCKET 5x2 | | | SSQ-105-24-F-D | Samtec | 5x2 100 mil |
| 19 | 1 | JS2 | CONN SOCKET 2x2/SM | | | SSM-102-L-DV-TR | Samtec | SMD 2x2 100mil |
| 20 | 1 | J1 | RJ-11 | | | 154-UL6641 | Mouser | thru-hole 6 |
| 23 | 2 | Q3,Q1 | NPN | | 300 V | MMBTA42LT1 | Motorola | SOT-23 |
| 24 | 1 | Q2 | PNP | | 300 V | MMBTA92LT1 | Motorola | SOT-23 |
| 25 | 2 | Q4,Q5 | NPN | | 80 V | MMBTA06LT1 | Motorola | SOT-23 |
| 29 | 1 | RV1 | SiDactor | 100 A | 275 V | P3100SB | Teccor | SOD 6 |
| 31 | 1 | R1 | 1.07 K | ±1% | 1/2 W | CR2010-2W-1071FT | Venkel | 2010 |
| 32 | 1 | R2 | 150 | ±5% | 1/16 W | CR0402-16W-150JT | Venkel | 402 |
| 33 | 1 | R3 | 3.65 K | ±1% | 1/2 W | CR2010-2W-3651FT | Venkel | 2010 |
| 34 | 1 | R4 | 2.49 K | ±1% | 1/2 W | CR2010-2W-2491FT | Venkel | 2010 |
| 35 | 2 | R6,R5 | 100 K | ±5% | 1/16 W | CR0402-16W-104JT | Venkel | 402 |
| 37 | 1 | R9 | 1 M | ±1% | 1/16 W | CR0402-16W-1004FT | Venkel | 402 |
| 38 | 1 | R10 | 536 | ±1% | 1/4 W | CR1206-4W-5360FT | Venkel | 1206 |
| 39 | 1 | R11 | 73.2 | ±1% | 1/2 W | CR2010-2W-73R2FT | Venkel | 2010 |
| 40 | 2 | R13,R12, R14 | 0 | ±1% | 1/16 W | CR0603-16W-000F | Venkel | 603 |
| 41 | 2 | R16,R15 | 0 | ±1% | 1/16 W | CR0805-16W-000F | Venkel | 805 |
| 42 | 2 | R32,R30 | 15M | ±5% | 1/8 W | CR0805-8W-156JT | Venkel | 805 |
| 43 | 2 | R31,R33 | 5.1M | ±5% | 1/8 W | CR0805-8W-515JT | Venkel | 805 |
| 45 | 1 | R75 | 47K | ±5% | 1/16 W | CR0603-16W-473JT | Venkel | 603 |
| 46 | 1 | R76 | 300 | ±5% | 1/16 W | CR0603-16W-301JT | Venkel | 603 |
| 47 | 2 | R80, R82 | 0 | ±5% | 1/16 W | CR0603-16W-000JT | Venkel | 603 |
| 54 | 3 | R300,R301,R302 | 0 | ±5% | 1/4 W | CR1206-4W-000JT | Venkel | 1206 |
| 55 | 1 | U1 | Si3050 | | | Si3050 | Silicon Labs | TSSOP 20 |
| 56 | 1 | U2 | Si3019 | | | Si3019 | Silicon Labs | TSSOP 16 |
| 58 | 1 | Z1 | 43 V | | 1/2 W | BZT52C43 | Diodes Inc. | SOD-123 |
| 59 | 6 | JP5 = "1"<br>JP6-JP9 = "Middle-Verticle"<br>JP10 = "/INT" | Jumpers | | | Standard Two Pin, 0.100" Jumpers | | n/a |

| No Install | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 11 | 1 | C90 | DNP 3.3 nF | ±10% | 16 V | C0603X7R160-332KNE | Venkel | 603 |
| 21 | 1 | LAH1 | DNP Logic Analyzer Header | | | 517-6121TN | Mouser | 10x2 100 mil |
| 22 | 1 | LS1 | DNP SPEAKER | | | BRT1209PF-06 | Intervox | Thru-Hole |
| 26 | 1 | Q10 | DNP MOSFET N GSD | | | FDV301N | Fairchild | SOT-23 |
| 27 | 2 | RF2,RF1 | DNP F1250T | | | F1250T | Teccor | FSOD6 |
| 28 | 1 | RL1 | DNP Opto-Relay | | | AQW210S | NAIS | SOIC 8 |
| 30 | 3 | RV3,RV4,RV5 | DNP SiDactor | 100 A | 275 V | P3100SB | Teccor | SOD 6 |
| 36 | 2 | R8,R7 | DNP 20 M | ±5% | 1/8 W | CR0805-8W-206JT | Venkel | 805 |
| 44 | 3 | R51,R52,R53 | DNP 47K | ±5% | 1/16 W | CR0603-16W-473JT | Venkel | 603 |
| 48 | 2 | R81, R83 | DNP 0 | ±5% | 1/16 W | CR0603-16W-000JT | Venkel | 603 |
| 49 | 1 | R90 | DNP 15k | ±5% | 1/10 W | CR0603-10W-511JT | Venkel | 603 |
| 50 | 1 | R101 | DNP 200 | ±5% | 2 W | CR2512-2W-201JT | Venkel | 2512 |
| 51 | 3 | R102,R103,R106 | DNP 1K | ±5% | 1/10 W | CR0805-10W-102JT | Venkel | 805 |
| 52 | 1 | R104 | DNP 1.5K | ±5% | 1/10 W | CR0805-10W-152JT | Venkel | 805 |
| 53 | 1 | R105 | DNP 10K | ±5% | 1/2 W | CR1210-2W-103JT | Venkel | 1210 |
| 57 | 1 | U3 | DNP Opto-Isolator | | | PS2501L-1 | NEC | GULL 6 |

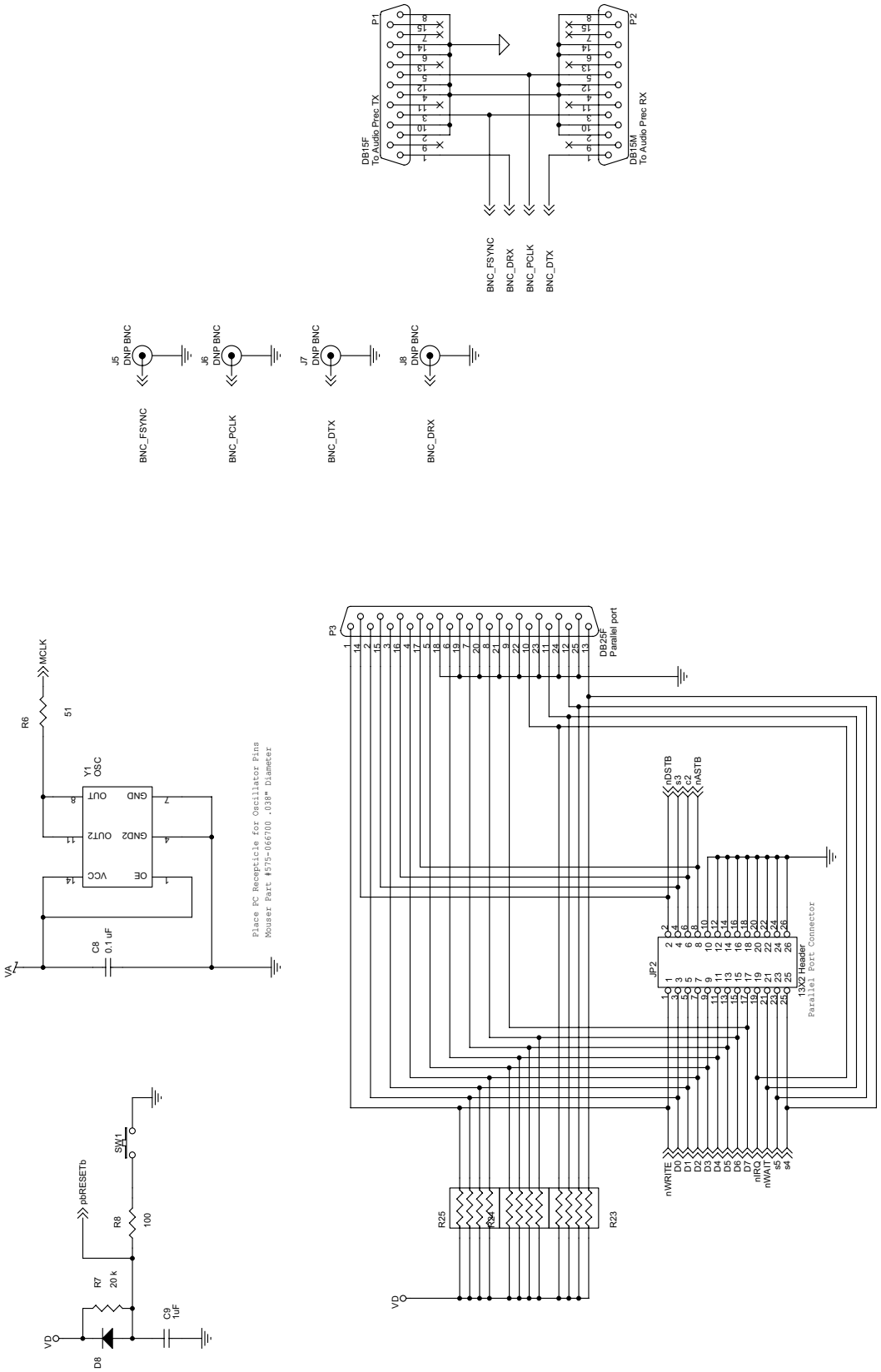



**Figure 14. Si3050-EVB Motherboard Typical Application Circuit (1 of 4)**

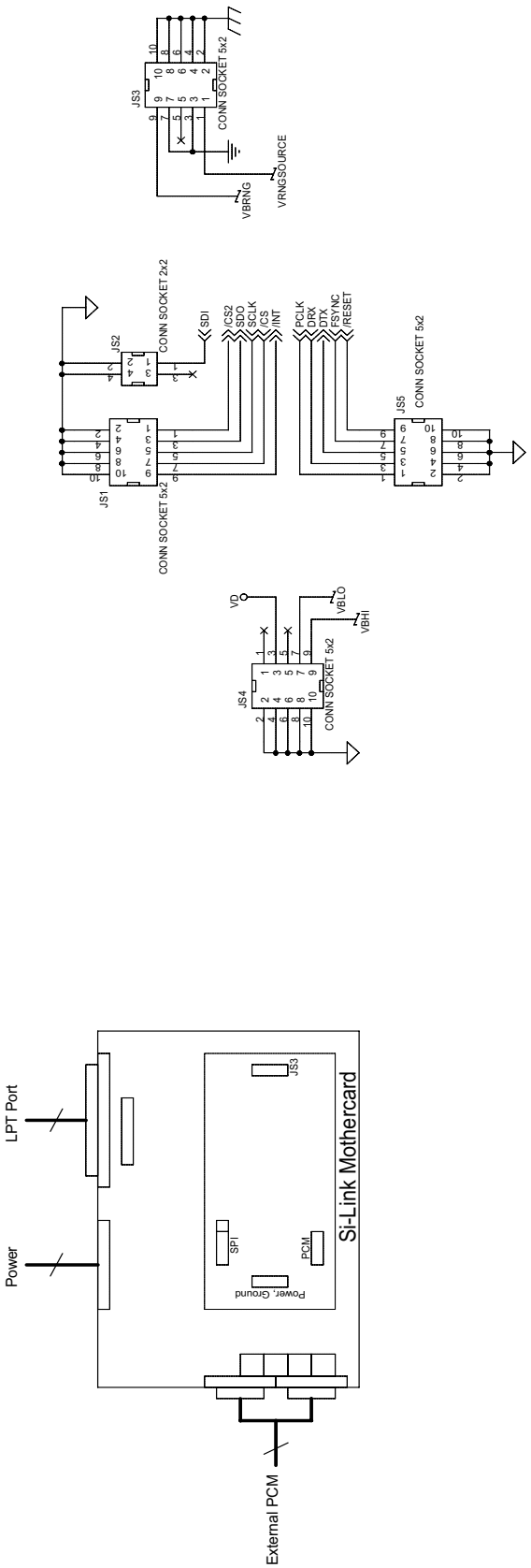



**Figure 15. Si3050-EVB Motherboard Typical Application Circuit (2 of 4)**

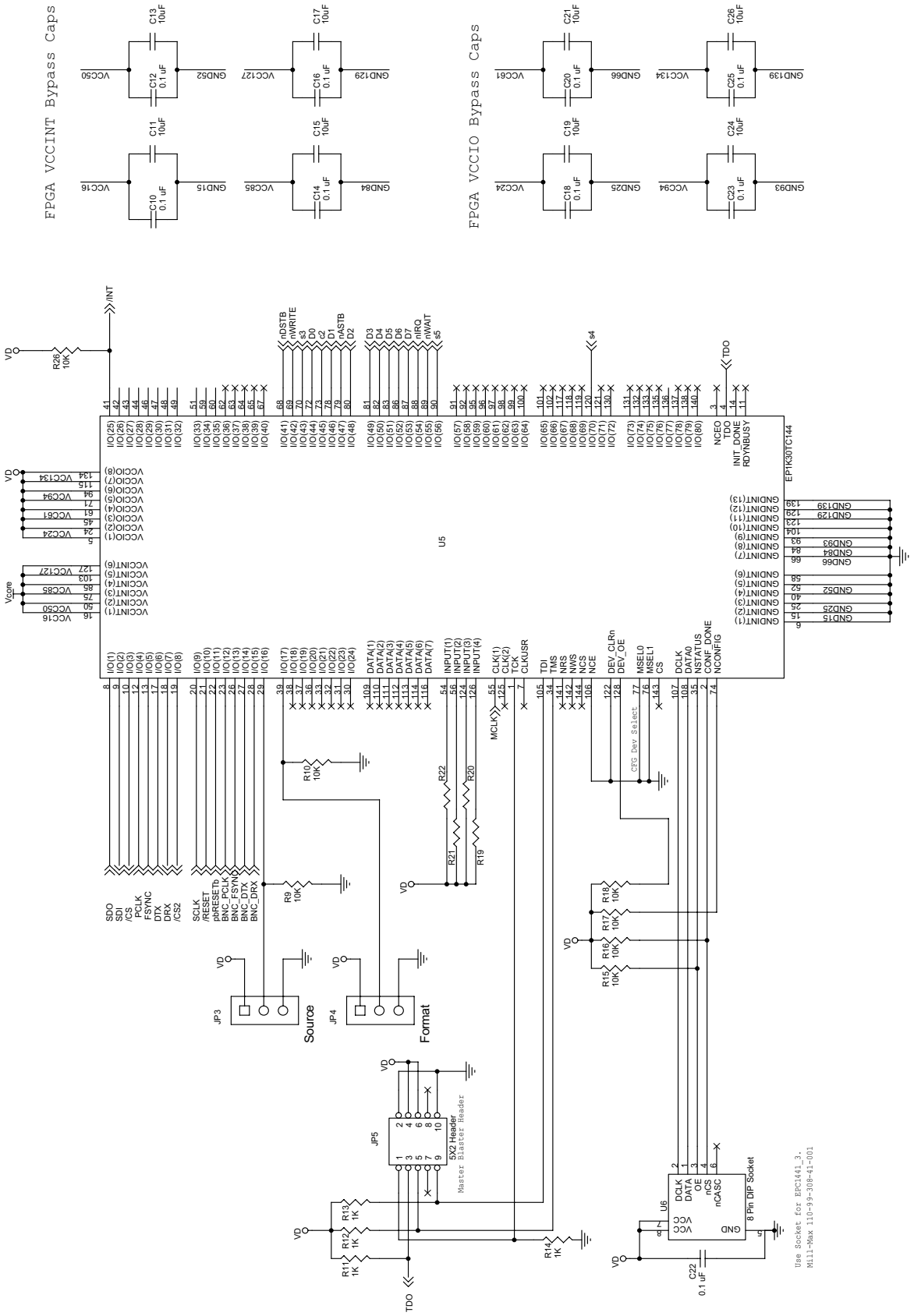



**Figure 16. Si3050-EVB Motherboard Typical Application Circuit (3 of 4)**

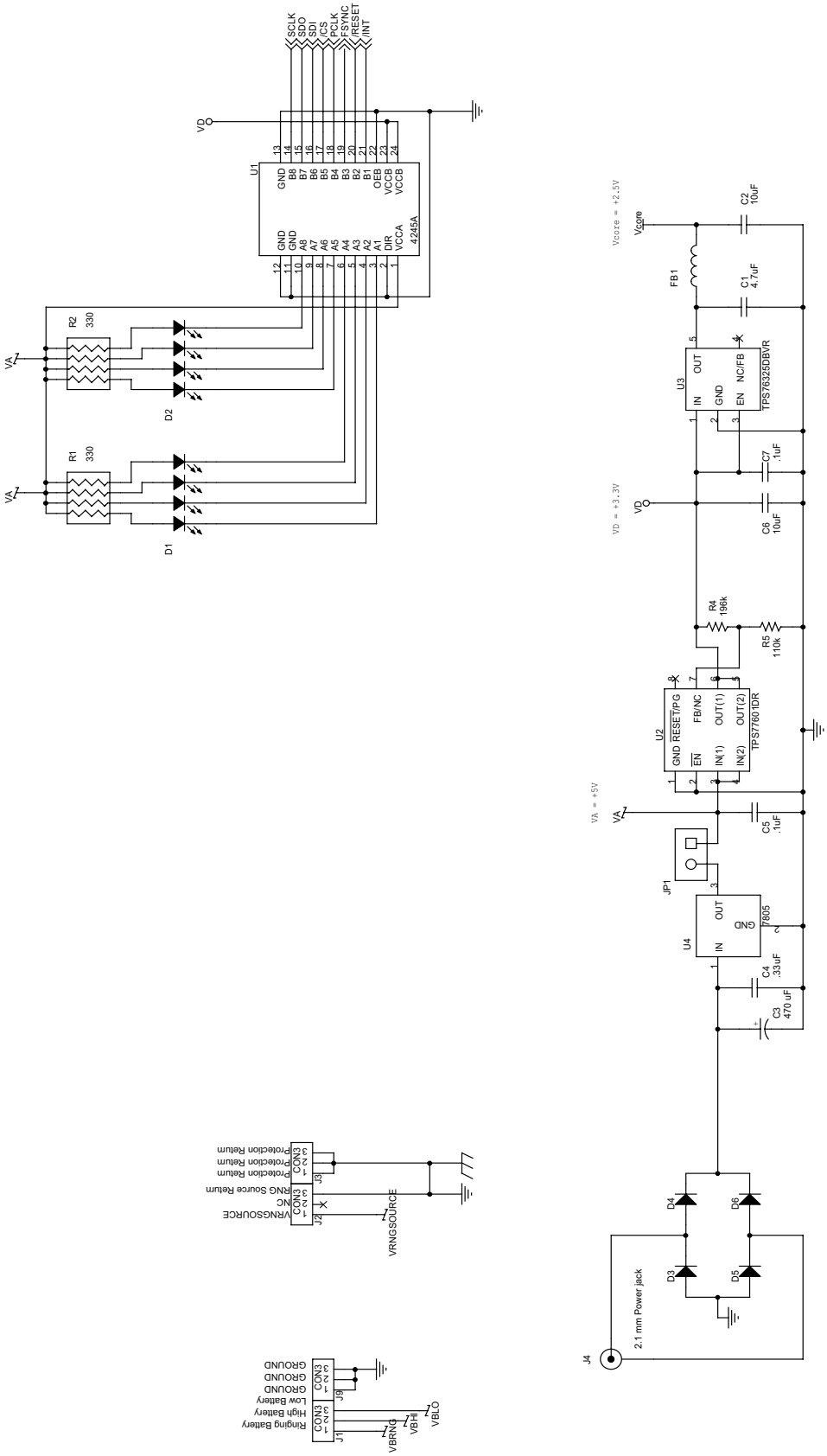



**Figure 17. Si3050-EVB Motherboard Typical Application Circuit (4 of 4)**

# 8. Bill of Materials: Si3050PPT-EVB Motherboard

| Reference | Value | Tolerance | Rating | Part Number | Manufacturer | PCB Footprint |
|---|---|---|---|---|---|---|
| C1 | 4.7uF | ±10% | 10V | C1206X7R100-475KNE | Venkel | SM/C_1206 |
| C2,C6,C11,C13,C15,C17, C19,C21,C24,C26 | 10uF | ±10% | 10 V | C1206X7R100-106KNE | Venkel | SM/C_1206 |
| C3 | 470 uF | ±20% | 25 V | NRSA471M25V10X16 | NIC Components | radial 10x16 |
| C4 | .33uF | ±10% | 10 V | C0805X7R250-334KNE | Venkel | SM/C_0805 |
| C5,C7 | .1uF | ±10% | 25V | C0805X7R250-104KNE | Venkel | SM/C_0805 |
| C8,C10,C12,C14,C16,C18, C20,C23,C25 | 0.1 uF | ±10% | 16 V | C0603X7R160-104KNE | Venkel | SM/C_0603 |
| C9 | 1uF | ±10% | 10 V | C1206X7R100-105KNE | Venkel | SM/C_1206 |
| C22 | 0.1 uF | ±10% | 16 V | C0603X7R160-104KNE | Venkel | 603 |
| D1,D2 | LED 4pack | | | SSF-LXH400ID | Lumex | |
| D3,D4,D5,D6 | DIODE | 0.5 A | 30 V | MBR0530T1 | Motorola | SOD-123 |
| D8 | DIODE | 75 V | 400 mA | 1N4148 | Diodes, Inc. | DO-35 |
| FB1 | Ferrite Bead on wire | | 3x1x4 (mm) | 2743015112 | Fair-Rite | thru-hole 2 |
| JP1 | 2X1 Header | | | 517-6111TN | Mouser | 2x1 100 mil |
| JP2 | 13X2 Header | | | 517-30326-6002 | Mouser | 13x2 100 mil |
| JP3,JP4 | 3X1 Header | | | 68000-403 | Berg | 3x1 100 mil |
| JP5 | 5X2 Header | | | 517-6121TN | Mouser | 5x2 100 mil |
| JS1,JS3,JS4,JS5 | CONN SOCKET 5x2 | | | SSW-105-01-T-D | Samtec | |
| JS2 | CONN SOCKET 2x2 | | | SSW-102-01-T-D | Samtec | |
| J1,J2,J3,J9 | CON3 | | | 2SV-03 | Thomas&Betts | |
| J4 | 2.1 mm Power jack | | | ADC-002-1 | Adam Tech | thru-hole 3 |
| J5,J6,J7,J8 | DNP BNC | | | 73133 | Molex | BNC |
| P1 | DB15F | | | 747845-4 | Amp | DB15 Female |
| P2 | DB15M | | | 747841-4 | Amp | DB15 Male |
| P3 | DB25F | | | 747846-3 | Amp | DB25 Female |
| R1,R2 | 330 | ±5% | 1/16 W | EXB-38V330JV | Panasonic | Resistor Pack |
| R4 | 196k | ±1% | 1/8 W | CR0805-8W-1963FT | Venkel | 805 |
| R5 | 110k | ±1% | 1/8 W | CR0805-8W-1103FT | Venkel | 805 |
| R6 | 51 | ±5% | 1/10 W | CR0805-10W-510JT | Venkel | 805 |
| R7 | 20 k | ±5% | 1/10 W | CR0805-10W-203JT | Venkel | 805 |
| R8 | 100 | ±5% | 1/4 W | CR1206-4W-473JT | Venkel | 1206 |
| R9,R10,R15,R16,R17,R18, R19,R20,R21,R22,R26 | 10K | ±5% | 1/16 W | CR0603-16W-103JT | Venkel | 603 |
| R11,R12,R13,R14 | 1K | ±5% | 1/16 W | CR0603-16W-102JT | Venkel | 603 |
| R23,R24,R25 | 220k | ±5% | 1/16 W | EXB-38V224JV | Panasonic | R-PAK |
| SW1 | SW PUSHBUTTON | | | 101-0161 | Mouser | thru-hole 4 |
| U1 | 4245A | | | SN74LVC4245A | TI | TSSOP-24 |
| U2 | TPS77601DR | | | TPS77601DR | Texas Instruments | 8-Pin SOIC |
| U3 | TPS76325DBVR | | | TPS76325DBVR | Texas Instruments | 5-Pin SOT-23 |
| U4 | 7805 | | | uA7805CKC | Texas Instruments | TO-220AB |
| U5 | EP1K30TC144 | | | EP1K30TC144-3 | Altera | TQFP-144 |
| U6 | 8 Pin DIP Socket | | | 110-99-308-41-001 | Mill-Max | 8-PIN PDIP |
| Y1 | OSC | | | SG-531PH | Epson | DIP14 |

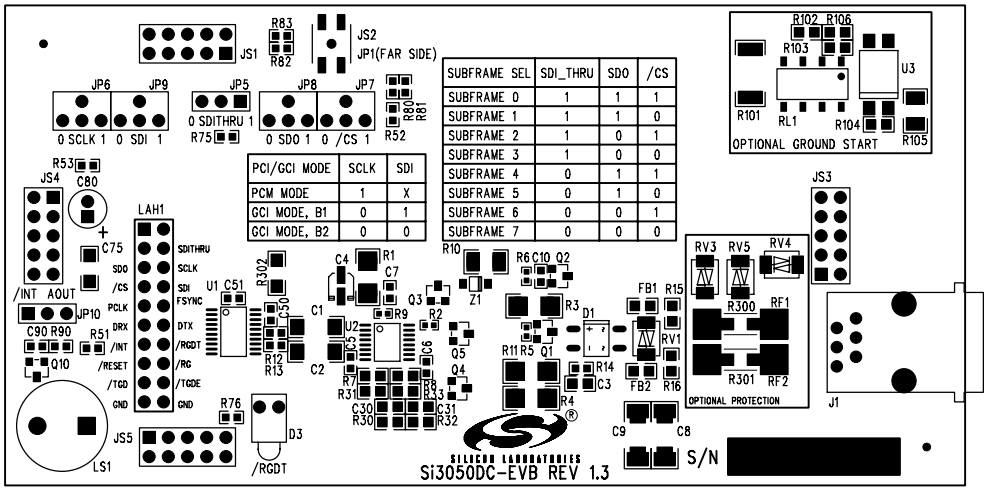



**Figure 18. Daughter Primary Assembly**

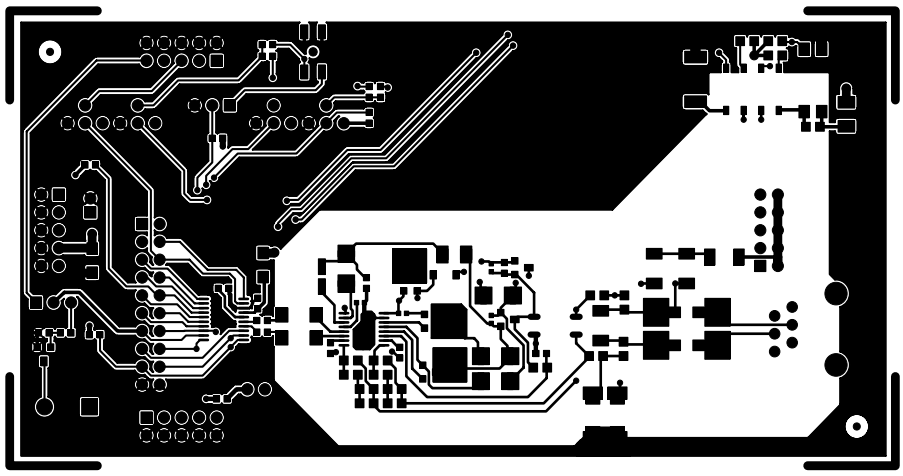


**Figure 19. Daughter Card Primary Side**

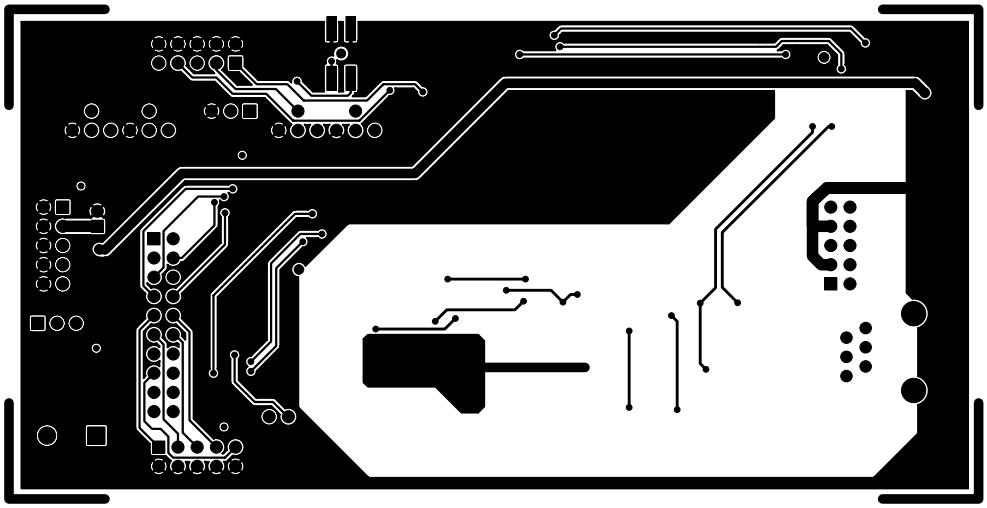


**Figure 20. Daughter Card Secondary Side**

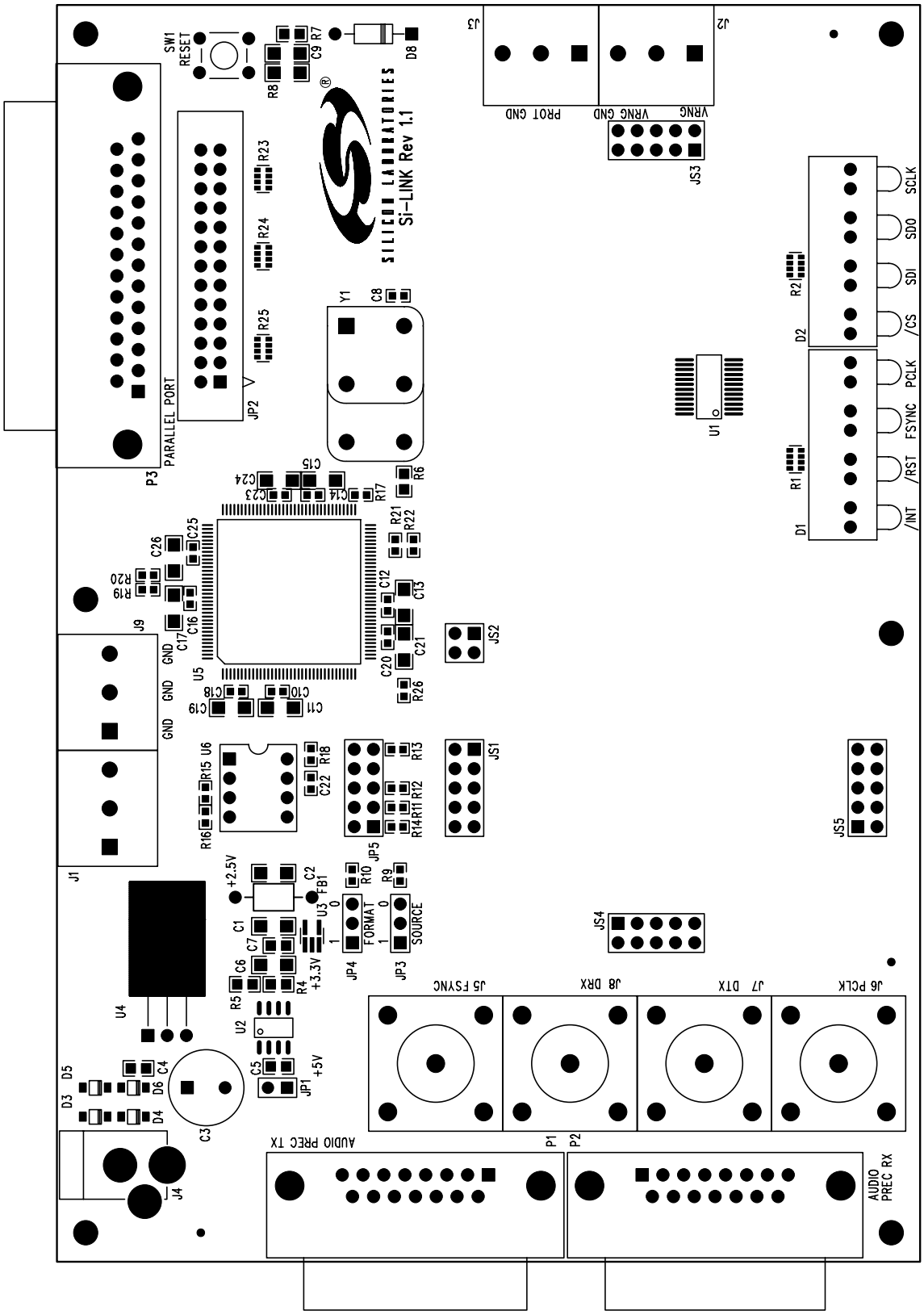



**Figure 21. Motherboard Primary Assembly**

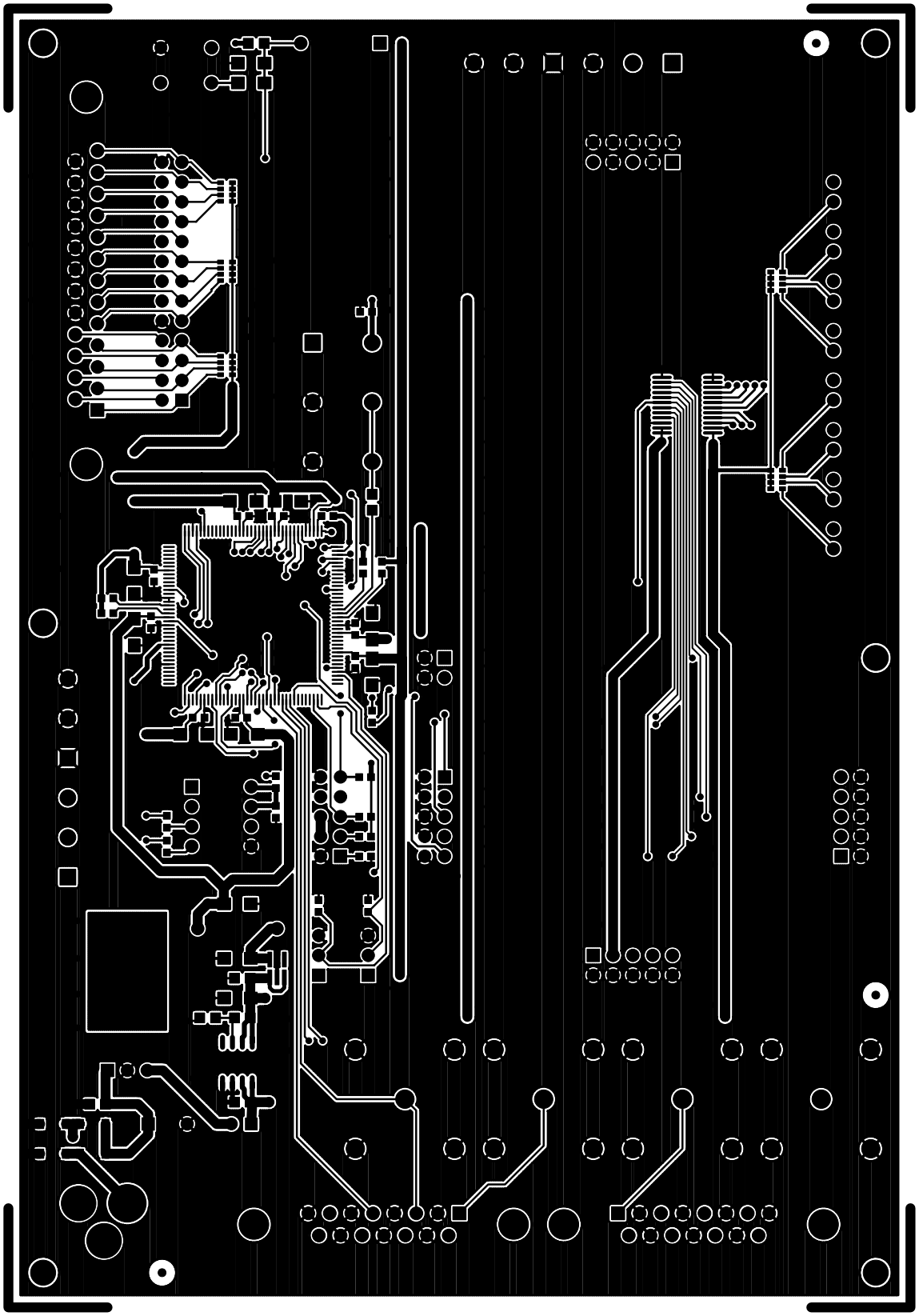


Figure 22. Motherboard Primary Side

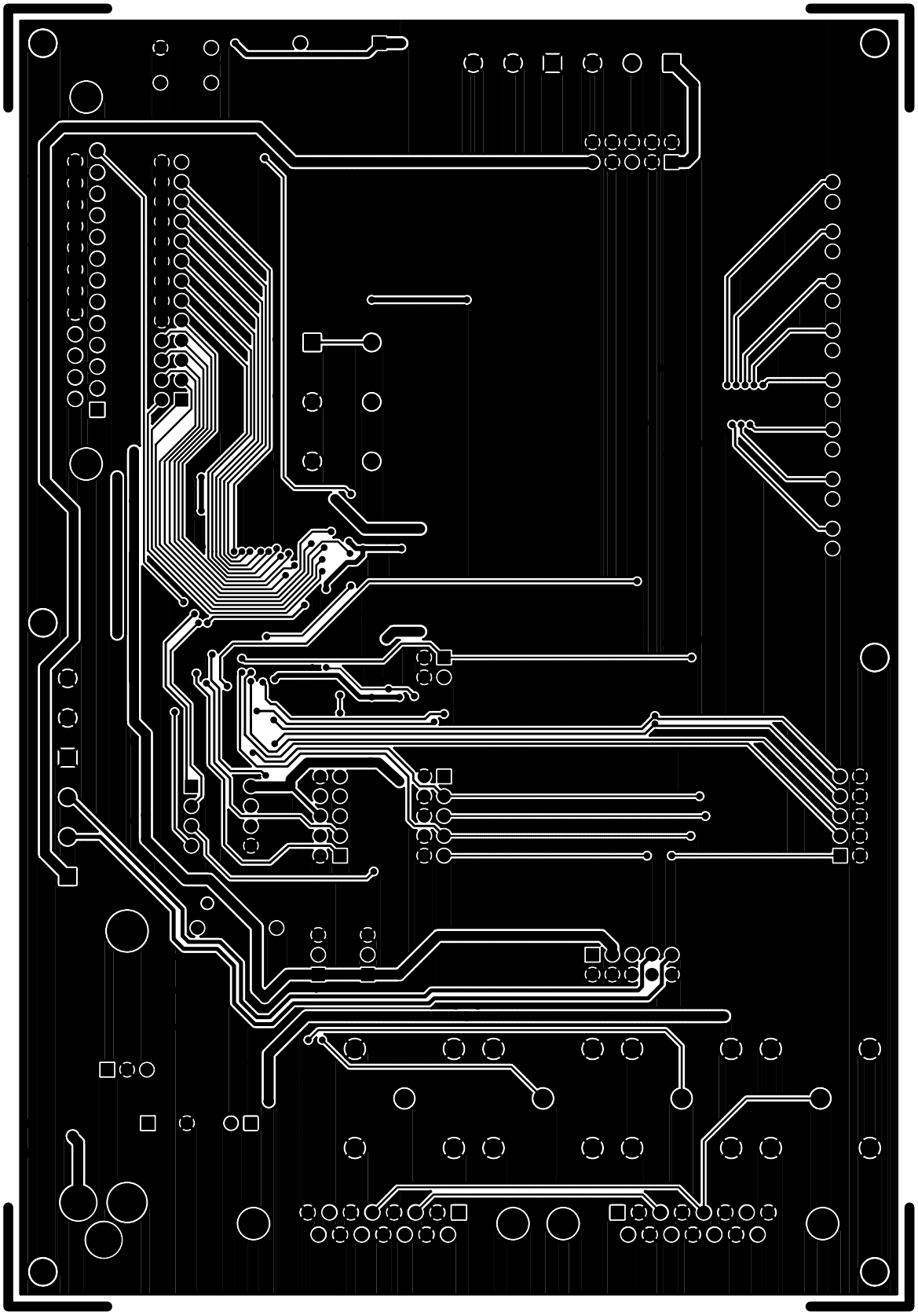


Figure 23. Motherboard Secondary Side

# DOCUMENT CHANGE LIST

## Revision 0.2 to Revision 0.3

- Updated schematics
- Updated BOMs
- Updated layers

## Revision 0.3 to Revision 0.4

- "1. Functional Description" on page 2: deleted text
- Table 3 moved
- Figure 4 updated
- Figure 8 updated
- "5.8. Si3019 Signal Path Control" on page 12: Added text.
- "5.9. Transhybrid Loss Calculation" on page 13 added.

## Revision 0.4 to Revision 1.0

- Updated Si3050 EVB schematics.
- Updated Si3050 EVB layout.
- Updated Si3050 EVB BOM.
- Added notification of support for Windows XP.
- Updated layout figure titles.

## NOTES:

## CONTACT INFORMATION

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